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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/739,388
Filing Date	December 19, 2000
First Named Inventor	Gene F. Young
Art Unit	2616
Examiner Name	Kevin C. Harper
Attorney Docket Number	42390P9956

Total Number of Pages in This Submission

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☒ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

-check for $620.00
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Paul A. Mendonsa, Reg. No. 42,879 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	December 14, 2006

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Typed or printed name	Katherine Jennings		
Signature		Date	December 14, 2006

FEE TRANSMITTAL for FY 2006

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	620.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

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☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	120.00
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify) _____					
				SUBTOTAL (2)	($) 620.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Paul A. Mendonsa	Registration No. (Attorney/Agent)	42,879	Telephone	(503) 439-8778
Signature				Date	12/14/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Young, Gene	Art Unit	: 2616
Serial No.	: 09/739,388	Examiner	: Harper, Kevin C
Filed	: 12/19/2000	Assignee	: Intel Corporation
Title	: HIGH DENSITY SERVERLETS UTILIZING A HIGH SPEED DATA BUS		

Mailstop **Appeal Briefs - Patents**
Commissioner for Patents
P.O. Box 1450
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Appeal Brief

(i) Real Party in Interest

The real party in interest in this appeal is Intel Corporation, a Delaware corporation having a principal place of business at 2200 Mission College Blvd, Santa Clara, CA 95052. Intel is the assignee of the entire right, title, and interest in the above-noted application.

(ii) Related appeals and interferences

None.

(iii) Status of claims

Claims 1-31 are pending and stand rejected. Applicant is appealing the rejection of all of claims 1-31.

(iv) Status of Amendments

No amendments were submitted after the Final Office Action mailed 06/15/2006.

(v) Summary of claimed subject matter

(a) Claim 1 recites a system module (e.g., FIG. 5, 100; page 9, lines 12-19) to couple a switch fabric network such as an Infiniband, Ethernet, or Fibrechannel network (e.g., page 10, line 2) to input/output (I/O) resources (e.g., FIG. 5, 182, 184; page 10, lines 17-19). The system module includes serverlets (e.g., FIG. 5, 112, 114) such as serverlets shown in FIG. 4 and described on page 8, line 11 - page 9, line 6. The system module includes a switching device (e.g., FIG. 5, 122; FIG. 7; page 10, lines 17-19; page 13, lines 10-page 15, line 7) to couple to each of the serverlets and to the I/O resources via a bus (e.g., FIG. 7, 340; page 14, lines 11-17). The module also includes another switching device (e.g., FIG. 5, 102; page 9, line 21- page 10, line 4) to couple to the switch fabric network and to the serverlets.

(b) Claim 11 recites a module (e.g., FIG. 5, 100; page 9, lines 12-19) that includes serverlets (e.g., FIG. 5, 112, 114, 116, 118) such as serverlets shown in FIG. 4 and described on page 8, line 11 - page 9, line 6. The module also includes a switching device (e.g., FIG. 5, 122; FIG. 7; page 10, lines 17-19; page 13, lines 10-page 15, line 7) to couple to input/output (I/O) resources (e.g., FIG. 5, 182, 184; page 10, lines 17-19) via a bus (e.g., FIG. 7, 340; page 14, lines 11-17). The module further includes a another switching device (e.g., FIG. 5, 102; page 9, line 21- page 10, line 4) to couple to the switch fabric network and to the first and second serverlets.

(c) Claim 20 recites a system that includes a switch fabric network (e.g., FIG. 1, 12; page 4, line 20-page 5, line 5), input/output (I/O) resources (e.g., FIG. 5, 182, 184; page 10, lines 17-19), and a module (e.g., FIG. 5, 100; page 9, lines 12-19) to couple said switch fabric network to said I/O resources. The module includes serverlets (e.g., FIG. 5, 112, 114) such as serverlets shown in FIG. 4 and described on page 8, line 11 - page 9, line 6. The module also includes a switching device (e.g., FIG. 5, 122; FIG. 7; page 10, lines 17-19; page 13, lines 10-page 15, line 7) to couple to each of said first serverlet and said second serverlet and to said I/O resources via a bus (e.g., FIG. 7, 340; page 14, lines 11-17) connecting the first switching device and the I/O resources such that said first serverlet and said second serverlet share said I/O resources. The module further includes another switching device (e.g., FIG. 5, 102; page 9, line 21-page 10, line 4) to couple to the switch fabric network and to the serverlets.

(d) Claim 25 recites a system that includes serverlets (e.g., FIG. 5, 112, 114, 116, 118). Each of the serverlets includes a processor (FIG. 4, 66; page 8, lines 14-17), at least one dual in-line memory module (e.g., FIG. 4, 52, 54, 56, 58; page 8, lines 14-17); and a power conversion unit (FIG. 4, 60; page 8, lines 14-17). The system also includes a chassis configured to house the multiple serverlets (page 10, lines 12-13). The chassis includes a switching device (e.g., FIG. 5, 122; FIG. 7; page 10, lines 17-19; page 13, lines 10-page 15, line 7) to couple the serverlets to at least one disk system shared by the serverlets via a bus (e.g., FIG. 7, 340; page 14, lines 11-17). The chassis also includes another switching device (e.g., FIG. 5, 102; page 9, line 21- page 10, line 4) to couple the serverlets to a switch fabric network.

(vi) Grounds of rejection to be reviewed on appeal

1. Whether independent claim 1 is unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

2. Whether independent claim 11 is unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

3. Whether independent claim 20 is unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

4. Whether independent claim 25 is unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Hipp et al. (U.S. 6,325,636) and Johnson et al. (U.S. 4,627,050)

(vii) Argument

(a) Whether claims 1-10 and 31 are unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

(1) Applicant disagrees that Chow discloses either the recited switch coupling serverlets to a switch fabric or the recited module

Independent claim 1 recites a module that includes a switch to couple serverlets to a switch fabric. The Examiner has rejected these claims based on a combination of Chow (U.S. 6,148, 349) and Matsunami (U.S. 6,542,961). In particular, the Examiner identified item 802 in FIG. 8 of Chow as the switch coupling the serverlets to a switch fabric. In particular, in the Advisory Action of 09/07/2006 the Examiner stated "the receive and send side interfaces each include only one processor for controlling communications. Therefore, several IONs and compute nodes are coupled to the fabric through each interface". Applicant however disagrees with this line of reasoning as it is inconsistent with the disclosure of Chow. That is, if the compute nodes and IONs each attach to the same processor as argued by the Examiner, why is there any need for the expensive and complexity of a switch fabric? If the Examiner's position were correct the processor could just deliver a message from one coupled compute node to an attached ION since it is directly coupled to both. Additionally, the illustration of FIG. 8 is at odds with the Examiner's interpretation. FIG. 8 shows each compute node and ION attaching to a different send side interface "box". For example, compute node A attaches to the

top send side interface box while ION 212 attaches to the bottom send side interface box. Additionally each box is shown as offering its own set of connections to switch nodes 812 which is consistent with each "box" representing a single send side interface. In a nutshell, since each ION connects to its own send side interface, the send side interface does not switch between ION nodes. Thus, item 802 in FIG. 8 of Chow does not provide the recited switch coupling the serverlets to a switch fabric

Additionally, over the course of prosecution, the Examiner changed the interpretation of the recited module to now feature a combination of ION clique 226 and the interface 802. However, if, as the Examiner argues, the same interface 802 is shared among IONs and compute nodes, how can ION clique 226 and interface 802 be considered a single module? That is, if ION clique 226 and interface 802 is one module, how do the other ION cliques 226 couple to the interface 802? More relevantly, what in Chow indicates that ION clique 226 and interface 802 form a module especially in view of Figure 1 that delineates storage resources 104 as separate from the BYNET and replicates the diagram of storage resources 104 multiple times. In short, Applicant disagrees that Chow discloses the recited module.

For at least the reasons above, Applicant requests withdrawal of the rejection of claim 1 and its corresponding dependent claims.

(2) Applicant disagrees that it would have been obvious to modify Chow in view of Matsunami in the manner proposed by the Examiner.

Applicant disagrees that it would have been obvious to modify Chow with the switches of Matsunami as proposed by the Examiner. In Chow, hosts 102 access storage via a BYNET Interconnect fabric 106. In Matsunami, hosts 30 access storage via diskarray switches 20. In other words, hosts 102 of Chow perform similar functions as the hosts 30 in Matsunami, namely initiating storage requests and processing the results. Similarly, both the BYNET fabric 106 and the diskarray switches 20 perform similar functions, namely, providing the hosts 102/30 with access to different storage components. The Examiner's proposed combination mixes and matches these components in a way that would not be obvious to one of skill in the art. In particular, the Examiner proposes interposing the diskarray switch 20 of Matsunami in between the I/O nodes 212, 214 and JBODs 222, 218 of Chow. However, in this combination, the diskarrays 20 of Matsunami are no longer coupled to hosts, ignoring the function played by the diskarray in Matsunami.

Additionally, the Examiner's proposed combination adds an additional stage to the task of servicing requests. That is, in the proposed combination, after finally traversing the BYNET fabric, a request in Chow runs into yet another switching stage (the proposed intermediate diskarray from Matsunami). In addition to further delay and additional logic, the proposed architecture is seemingly unnecessary. In Chow, scalability is provided by the BYNET fabrics 106. That is, adding additional resources

consistent with Chow, is simply a matter of attaching more nodes and JBODs 222, 224 to one of the fabrics.

Finally, as described in Matsunami, the Diskarray switch features a crossbar switch. The Examiner proposes using the crossbar switch in the proposed combination to create a path connecting a JBOD to IONs. During the period of time a path is made between a JBOD and an ION, due to the conventional blocking nature of a crossbar switch, the other ION is excluded from accessing the particular JBOD. Chow emphasizes that "at any given time both IONs 212 and 214 in a dipole 226 must be able to access all devices" (col. 8, lines 63-67). Chow achieves this continuous access by providing each ION with direct dedicated connections with each JBOD (see FIG. 1 of Chow). The use of Matsunami's crossbar switch would undermine this important aspect of Chow. That is, the IONs would not be able to access all devices at any given time. Instead the use of a crossbar switch would force a given ION to wait to access a JBOD until the needed path through the crossbar switch was available.

Thus, for at least the reasons above, Applicant disagrees that one of skill in the art would combine Chow and Matsunami in the manner proposed by the Examiner. Applicant respectfully requests withdrawal of claim 1 and its corresponding dependent claims for at least these reasons.

(b) Whether claims 11-19 are unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

(1) Applicant disagrees that Chow discloses the recited switch coupling serverlets to a switch fabric or the recited module

Independent claim 11 recites a module that includes a switch to couple serverlets to a switch fabric. The Examiner has rejected these claims based on a combination of Chow (U.S. 6,148, 349) and Matsunami (U.S. 6,542,961). In particular, the Examiner identified item 802 in FIG. 8 of Chow as the switch coupling the serverlets to a switch fabric. In particular, in the Advisory Action of 09/07/2006 the Examiner stated "the receive and send side interfaces each include only one processor for controlling communications. Therefore, several IONs and compute nodes are coupled to the fabric through each interface". Applicant however disagrees with this line of reasoning as it is inconsistent with the disclosure of Chow. That is, if the compute nodes and IONs each attach to the same processor as argued by the Examiner, why is there any need for the expensive and complexity of a switch fabric? If the Examiner's position were correct the processor could just deliver a message from one coupled compute node to an attached ION since it is directly coupled to both. Additionally, the illustration of FIG. 8 is at odds with the Examiner's interpretation. FIG. 8 shows each compute node and ION attaching to a different send side interface "box". For example, compute node A attaches to the top send side interface box while ION 212 attaches to the bottom send side interface box. Additionally each box is shown as offering its own set of connections to switch nodes 812 which is consistent with each "box" representing a single send side interface. In a nutshell, since each ION connects to its own send side interface, the send side

interface does not switch between ION nodes. Thus, item 802 in FIG. 8 of Chow does not provide the recited switch coupling the serverlets to a switch fabric

Additionally, over the course of prosecution, the Examiner changed the interpretation of the recited module to now feature a combination of ION clique 226 and the interface 802. However, if, as the Examiner argues, the same interface 802 is shared among several IONs and compute nodes, how can ION clique 226 and interface 802 be considered a single module? That is, if ION clique 226 and interface 802 is one module, how do the other ION cliques 226 couple to the interface 802? More relevantly, what in Chow indicates that ION clique 226 and interface 802 form a module especially in view of Figure 1 that delineates storage resources 104 as separate from the BYNET and replicates the diagram of storage resources 104 multiple times. In short, Applicant disagrees that Chow discloses the recited module.

For at least the reasons above, Applicant requests withdrawal of the rejection of claim 11 and its corresponding dependent claims.

(2) Applicant disagrees that it would have been obvious to modify Chow in view of Matsunami in the manner proposed by the Examiner.

Applicant disagrees that it would have been obvious to modify Chow with the switches of Matsunami as proposed by the Examiner. In Chow, hosts 102 access storage via a BYNET Interconnect fabric 106. In Matsunami, hosts 30 access storage via diskarray switches 20. In other words, hosts 102 of Chow perform similar functions as the hosts 30 in Matsunami, namely initiating storage requests and processing the

results. Similarly, both the BYNET fabric 106 and the diskarray switches 20 perform similar functions, namely, providing the hosts 102/30 with access to different storage components. The Examiner's proposed combination mixes and matches these components in a way that would not be obvious to one of skill in the art. In particular, the Examiner proposes interposing the diskarray switch 20 of Matsunami in between the I/O nodes 212, 214 and JBODs 222, 218 of Chow. However, in this combination, the diskarrays 20 of Matsunami are no longer coupled to hosts, ignoring the roles played by the Diskarrays and BYNET in their respective patents.

Additionally, the Examiner's proposed combination adds an additional stage to the task of servicing requests. That is, in the proposed combination, after finally traversing the BYNET fabric, a request in Chow runs into yet another switching stage (the proposed intermediate diskarray from Matsunami). In addition to further delay and additional logic, the proposed architecture is seemingly unnecessary. In Chow, scalability is provided by the BYNET fabrics 106. That is, adding additional resources, consistent with Chow, is simply a matter of attaching more nodes and JBODs 222, 224 to one of the fabrics.

Finally, as described in Matsunami, the Diskarray switch features a crossbar switch. The Examiner proposes using the crossbar switch in the proposed combination to create a path connecting a JBOD to an ION. During the period of time a path is made between JBOD and ION, due to the conventional blocking nature of a crossbar switch, the other ION is excluded from accessing the particular JBOD. Chow emphasizes that "at any given time both IONs 212 and 214 in a dipole 226 must be able to access all devices" (col. 8, lines 63-67). Chow achieves this continuous access by

providing each ION with direct dedicated connections with each JBOD (see FIG. 1 of Chow). The use of Matsunami's crossbar switch would undermine this important aspect of Chow. That is, the IONs would not be able to access all devices at any given time. Instead delays due to operation of the crossbar switch would force a given ION to wait to access a JBOD until the needed path through the crossbar switch was available.

Thus, for at least the reasons above, Applicant disagrees that one of skill in the art would combine Chow and Matsunami in the manner proposed by the Examiner. Applicant respectfully requests withdrawal of claim 11 and its corresponding dependent claims for at least these reasons.

(c) Whether claims 20-24 are unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Matsunami et al. (U.S. 6,542,961).

(1) Applicant disagrees that Chow discloses the recited switch coupling serverlets to a switch fabric or the recited module

Independent claim 20 recites a module that includes a switch to couple serverlets to a switch fabric. The Examiner has rejected these claims based on a combination of Chow (U.S. 6,148, 349) and Matsunami (U.S. 6,542,961). In particular, the Examiner identified item 802 in FIG. 8 of Chow as the switch coupling the serverlets to a switch fabric. In particular, in the Advisory Action of 09/07/2006 the Examiner stated "the receive and send side interfaces each include only one processor for controlling communications. Therefore, several IONs and compute nodes are coupled to the fabric

through each interface". Applicant however disagrees with this line of reasoning as it is inconsistent with the disclosure of Chow. That is, if the compute nodes and IONs each attach to the same processor as argued by the Examiner, why is there any need for the expensive and complexity of a switch fabric? If the Examiner's position were correct the processor could just deliver a message from one coupled compute node to an attached ION since it is directly coupled to both. Additionally, the illustration of FIG. 8 is at odds with the Examiner's interpretation. FIG. 8 shows each compute node and ION attaching to a different send side interface "box". For example, compute node A attaches to the top send side interface box while ION 212 attaches to the bottom send side interface box. Additionally each box is shown as offering its own set of connections to switch nodes 812 which is consistent with each "box" representing a single send side interface. In a nutshell, since each ION connects to its own send side interface, the send side interface does not switch between ION nodes. Thus, item 802 in FIG. 8 of Chow does not provide the recited switch coupling the serverlets to a switch fabric

Additionally, over the course of prosecution, the Examiner changed the interpretation of the recited module to now feature a combination of ION clique 226 and the interface 802. However, if, as the Examiner argues, the same interface 802 is shared among several IONs and compute nodes, how can ION clique 226 and interface 802 be considered a single module? That is, if ION clique 226 and interface 802 is one module, how do the other ION cliques 226 couple to the interface 802? More relevantly, what in Chow indicates that ION clique 226 and interface 802 form a module especially in view of Figure 1 that delineates storage resources 104 as separate from the BYNET

and replicates the diagram of storage resources 104 multiple times. In short, Applicant disagrees that Chow discloses the recited module.

For at least the reasons above, Applicant requests withdrawal of the rejection of claim 20 and its corresponding dependent claims.

(2) Applicant disagrees that it would have been obvious to modify Chow in view of Matsunami in the manner proposed by the Examiner.

Applicant disagrees that it would have been obvious to modify Chow with the switches of Matsunami as proposed by the Examiner. In Chow, hosts 102 access storage via a BYNET Interconnect fabric 106. In Matsunami, hosts 30 access storage via diskarray switches 20. In other words, hosts 102 of Chow perform similar functions as the hosts 30 in Matsunami, namely initiating storage requests and processing the results. Similarly, both the BYNET fabric 106 and the diskarray switches 20 perform similar functions, namely, providing the hosts 102/30 with access to different storage components. The Examiner's proposed combination mixes and matches these components in a way that would not be obvious to one of skill in the art. In particular, the Examiner proposes interposing the diskarray switch 20 of Matsunami in between the I/O nodes 212, 214 and JBODs 222, 218 of Chow. However, in this combination, the diskarrays 20 of Matsunami are no longer coupled to hosts, ignoring the roles played by the Diskarrays and BYNET in their respective patents.

Additionally, the Examiner's proposed combination adds an additional stage to the task of servicing requests. That is, in the proposed combination, after finally

traversing the BYNET fabric, a request in Chow runs into yet another switching stage (the proposed intermediate diskarray from Matsunami). In addition to further delay and additional logic, the proposed architecture is seemingly unnecessary. In Chow, scalability is provided by the BYNET fabrics 106. That is, adding additional resources, consistent with Chow, is simply a matter of attaching more nodes and JBODs 222, 224 to one of the fabrics.

Finally, as described in Matsunami, the Diskarray switch features a crossbar switch. The Examiner proposes using the crossbar switch in the proposed combination to create a path connecting a JBOD to an ION. During the period of time a path is made between JBOD and ION, due to the conventional blocking nature of a crossbar switch, the other ION is excluded from accessing the particular JBOD. Chow emphasizes that "at any given time both IONs 212 and 214 in a dipole 226 must be able to access all devices" (col. 8, lines 63-67). Chow achieves this continuous access by providing each ION with direct dedicated connections with each JBOD (see FIG. 1 of Chow). The use of Matsunami's crossbar switch would undermine this important aspect of Chow. That is, the IONs would not be able to access all devices at any given time. Instead delays due to operation of the crossbar switch would force a given ION to wait to access a JBOD until the needed path through the crossbar switch was available.

Thus, for at least the reasons above, Applicant disagrees that one of skill in the art would combine Chow and Matsunami in the manner proposed by the Examiner. Applicant respectfully requests withdrawal of claim 20 and its corresponding dependent claims for at least these reasons.

(d) Whether claims 25-30 are unpatentable under 35. U.S.C. s. 103 over Chow et al. (U.S. 6,148,349) in view of Hipp et al. (U.S. 6,325,636) and Johnson et al. (U.S. 4,627,050)

Claim 25 recites a system that includes multiple serverlets and a chassis that includes "a first switching device to couple the serverlets to at least one disk system shared by the serverlets via a bus connecting the first switching device and the at least one disk system ". The Examiner states that Chow in view of Hipp does not disclose a first switch coupled to a data bus. The Examiner argues that it would have been obvious to one of skill in the art to add the intershelf bus (item 10) expander (item 11) of Johnson to Chow/Hipp to provide the recited "first switching device". Though the Examiner referred to FIG. 2 in the Final Office Action mailed 06/15/06, presumably, the Examiner meant FIG. 1 as FIG. 2 does not include an item 11 nor a bus 10. In any event, Applicant disagrees with the Examiner's position in many regards.

First, bus 10 is not a bus 10 that connects either line cards 15 or shelf bus 12 to a disk system as recited by claim 25. Instead bus 10 provides a shared bus between intershelf expanders 11 and a TDM controller circuit 17. Secondly, in Johnson, the expander 11 and bus 10 are part of a system that delivers data between peer line-cards 15 on different shelves. Using an expander 11 and bus 10 to establish peer-to-peer data delivery from one ION to another ION would not provide a switch device that connects serverlets to at least one disk system by a bus. Finally, the Examiner does not provide a motivation to change Chow's data access system to a Time Division Multiplex system. A TDM system is used in Johnson because Johnson describes a

telephone branch exchange where TDM is commonly used. The Examiner, however, does not provide a motivation to alter the storage scheme Chow into a TDM architecture.

Finally, the motivation offered for combining Chow with Johnson is to "provide increased throughput for connected modules" citing col. 1, lines 21-25 and col. 2 lines 35-38 of Johnson. These passages of Johnson, however, allude to the advantage of using a pair of unidirectional buses (FIG. 2, items 27 and 29) over a single bidirectional bus (FIG. 1, item 10) in a branch exchange. The Examiner has not provided an explanation of why Johnson's splitting of a bidirectional bus into a unidirectional busses in a branch exchange would lead one of skill in the art to provide an shelf expander 11 into the system of Chow.

For at least these reasons, Applicant request withdrawal of the rejection of claim 25 and its corresponding dependent claims.

(viii) Claims appendix

1. A system module to couple a switch fabric network to input/output (I/O) resources, said system module comprising:

a first serverlet;

a second serverlet;

a first switching device to couple to each of said first serverlet and said second serverlet and to said I/O resources via a bus connecting the first switching device and the I/O resources such that said first serverlet and said second serverlet share said I/O resources; and

a second switching device to couple to the switch fabric network and to the first and second serverlets.

2. The system module of claim 1, wherein said I/O resources comprise a first disk system and a second disk system.

3. The system module of claim 1, wherein the first serverlet comprises first memory devices, a first processing unit, a first power conversion unit and a first interfacing unit to couple said first processing unit to said first memory devices.

4. The system module of claim 3, wherein the second serverlet comprises second memory devices, a second processing unit, a second power conversion unit and

a second interfacing unit to couple said second processing unit to said second memory devices.

5. The system module of claim 1, wherein the switch fabric network comprises one of an Infiniband network, an Ethernet network and a Fibre Channel network.

6. The system module of claim 1, further comprising a data bus to couple said first serverlet to said first switching device and to couple said second serverlet to said first switching device.

7. The system module of claim 1, further comprising a third switching device to couple to said switch fabric network, and a data bus to couple said first serverlet to said second and third switching devices and to couple said second serverlet to said second and third switching devices.

8. The system module of claim 7, wherein said second switching device comprises a first conversion unit to couple to said data bus, a second conversion unit to couple to said data bus, and a switching device to couple to said switch fabric network and to each of said first conversion unit and said second conversion unit.

9. The system module of claim 1, wherein said first switching device comprises:

a first interface device to couple to said first serverlet;

a second interface device to couple to said second serverlet;

a switching device to couple to said first interface device and said second interface device; and

a controller device to couple to said switching device and to a data bus that is coupled to said I/O resources.

10. The system module of claim 9, further comprising a third interface device to couple between said controller device and said data bus.

11. A module comprising:

a plurality of serverlets;

a first switching device to couple to input/output (I/O) resources via a bus connecting the first switching device and the I/O resources and to couple to said plurality of serverlets such that said plurality of serverlets share said I/O resources; and

a second switching device to couple to the switch fabric network and to the first and second serverlets.

12. The module of claim 11, wherein said I/O resources comprise a first disk system and a second disk system.

13. The module of claim 11, wherein each of said plurality of serverlets separately comprise memory devices, a processing unit, a power conversion unit and an interfacing unit to couple said processing unit to said memory devices.

14. The module of claim 11, wherein said module is coupled to a switch fabric network, said switch fabric network comprising one of an Infiniband network, an Ethernet network and a Fibre Channel network.

15. The module of claim 11, further comprising a data bus to couple said plurality of serverlets to said first switching device.

16. The module of claim 11, further comprising a third switching device to couple to said switch fabric network, and a data bus to couple said plurality of serverlets to said second and third switching devices.

17. The module of claim 16, wherein said second switching device comprises a first conversion unit to couple to said data bus, a second conversion unit to couple to said data bus, and a switching device to couple to said switch fabric network and to each of said first conversion unit and said second conversion unit.

18. The module of claim 11, wherein said first switching device comprises:

a first interface device to couple to a first one of said plurality of serverlets;

a second interface device to couple to a second one of said plurality of serverlets;

a switching device to couple to said first interface device and said second interface device; and

a controller device to couple to said switching device and to a data bus that is coupled to said I/O resources.

19. The module of claim 18, further comprising a third interface device to couple between said controller device and said data bus.

20. A system comprising:

a switch fabric network;

input/output (I/O) resources; and

a module to couple said switch fabric network to said I/O resources, said module comprising:

a first serverlet;

a second serverlet;

a first switching device to couple to each of said first serverlet and said second serverlet and to said I/O resources via a bus connecting the first switching device and the I/O resources such that said first serverlet and said second serverlet share said I/O resources; and

a second switching device to couple to the switch fabric network and to the first and second serverlets.

21. The system of claim 20, wherein said I/O resources comprise a first disk system and a second disk system.

22. The system of claim 20, wherein the switch fabric network comprises one of an Infiniband network, an Ethernet network and a Fibre Channel network.

23. The system of claim 20, further comprising a third switching device to couple to said switch fabric network, said data bus to couple said first serverlet to said second and third switching devices and to couple said second serverlet to said second and third switching devices.

24. The system of claim 23, wherein said second switching device comprises a first conversion unit to couple to said data bus, a second conversion unit to couple to said data bus, and a switching device to couple to said switch fabric network and to each of said first conversion unit and said second conversion unit.

25. A system, comprising:

(1) multiple serverlets, each of the serverlets comprising:

a processor;

at least one dual in-line memory module; and

a power conversion unit; and

(2) a chassis configured to house the multiple serverlets, the chassis comprising:

a first switching device to couple the serverlets to at least one disk system shared by the serverlets via a bus connecting the first switching device and the at least one disk system; and

a second switching device to couple the serverlets to a switch fabric network.

26. The system of claim 25, wherein a first data bus coupling the first switching device and a second data bus coupling the serverlets and the second switching device comprise the same type of data busses.

27. The system of claim 26, wherein the data busses comprise hublink data busses.

28. The system of claim 25, wherein the serverlets access the at least one disk system to access boot information.

29. The system of claim 25, wherein each of the serverlets do not include a cooling system.

30. The system of claim 25, wherein each of the serverlets do not include an internal disk system.

31. The system module of claim 1, wherein the first switching device comprises a many-to-one switching device to couple the plurality of serverlets to a single bus interface.

(ix) Evidence appendix

None

(x) Related proceedings appendix

None

Respectfully submitted,

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